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Jameco Part Number 26147

ORIGINAL 26147 → 26139

December 1980

MM54104 DIGITALKER™ Speech Synthesis System

General Description

The DIGITALKER is a speech synthesis system consisting of multiple N-channel MOS integrated circuits. It contains an MM54104 speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed. This can be expanded with minimal external logic.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

Encoding (digitizing) of custom word or phrase lists must be done by National Semiconductor. Customers submit to the factory high quality recorded magnetic reel to reel tapes containing the words or phrases to be encoded. National Semiconductor will sell kits consisting of the SPC and ROM(s) containing the digitized word or phrases.

Features

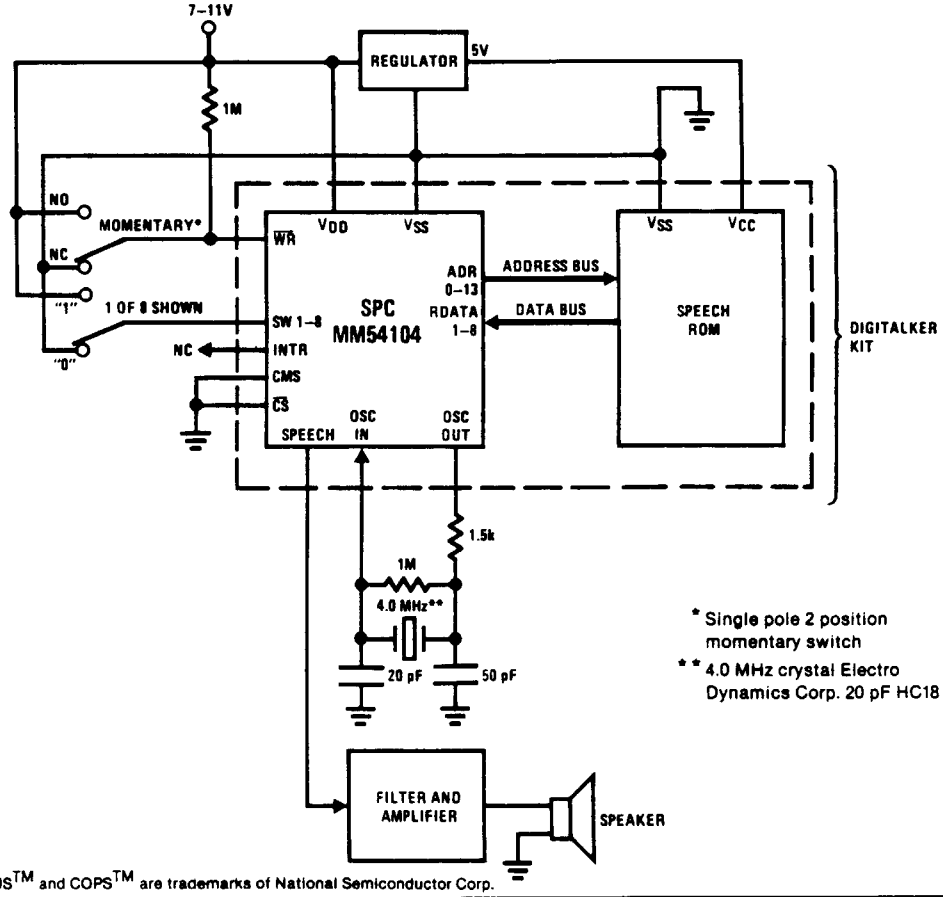
- Designed to be easily interfaced to most popular microprocessors
- 256 possible addressable expressions
- Male, female, and children's voices
- Any language
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- MICROBUS™ and COPS™ compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Easily expandable to greater than 128k ROM
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Ability to store silence durations for timing sequences

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. 20 pF HC18

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IM-FL30M120/Printed in U.S.A.

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C	Voltage at Any Pin	12V
Operating Temperature Range	−40°C to 85°C	Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
V_{DD}-V_{SS}	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 0°C$ to 70°C, $V_{DD} = 7V$-11V, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IL}	Input Low Voltage	$T_A = -40°C$ to 85°C	−0.3		0.6	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IH}	Input High Voltage	$T_A = -40°C$ to 85°C	2.2		V_{DD}	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\ \mu A$	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
V_{OLX}	Clock Output Low Voltage	Typical Crystal Configuration and 10M Load on Pin 2			1.2	V
V_{OHX}	Clock Output High Voltage	Typical Crystal Configuration and 10M Load on Pin 2	5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{DD}	Power Supply Current	$T_A = -40°C$ to 85°C			50	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			0.45 V_{DD}		V
V_{OUT}	Peak to Peak Speech Output	$V_{DD} = 11V$		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

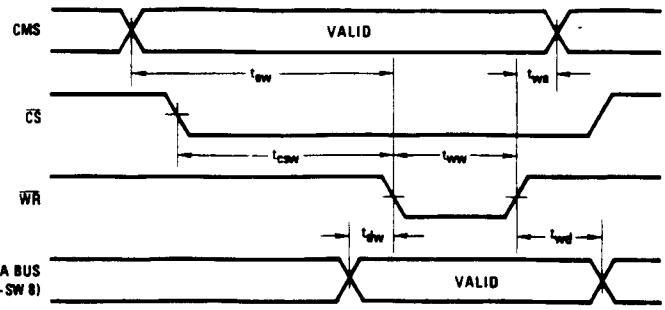
AC Electrical Characteristics $T_A = 0°C$ to 70°C, $V_{DD} = 7V$-11V, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{red}	$\overline{\text{ROMEN}}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

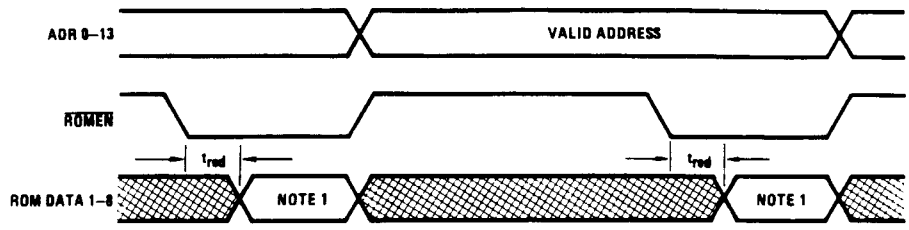
Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.

Timing Waveforms

Command Sequence



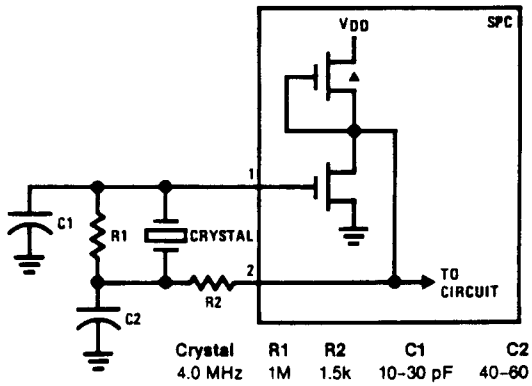
ROM Data Timing



Note 1: ROM data 1-8 can go valid any time after ADR 0-13 changes, however it must be valid within the t_{red} specifications and remain valid until $\overline{ROMEN}$ goes high.

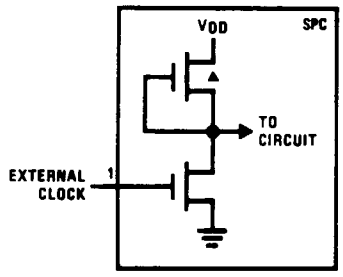
Crystal Circuit Information

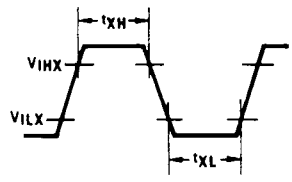
Typical Crystal Oscillator Network



Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10-30 pF	40-60 pF

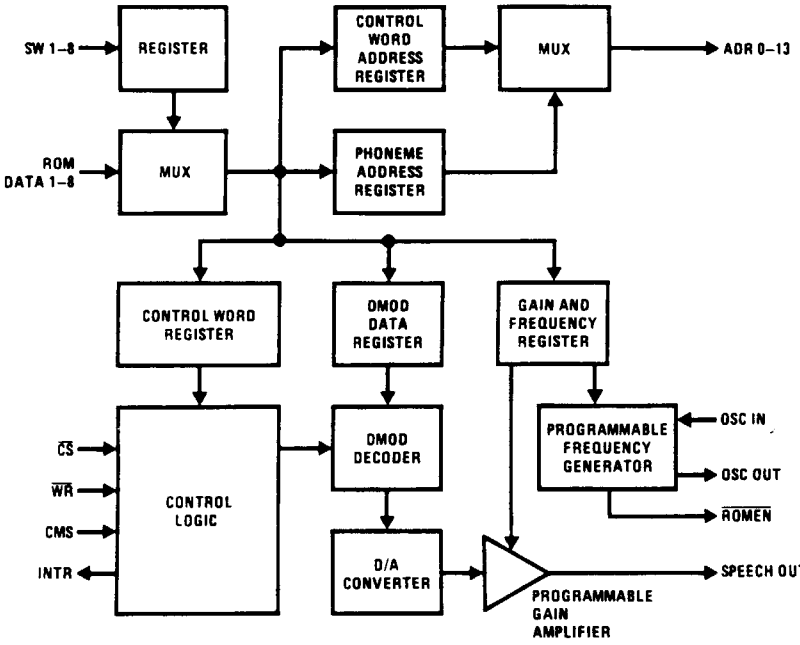
External Clock Input (4.0 MHz)



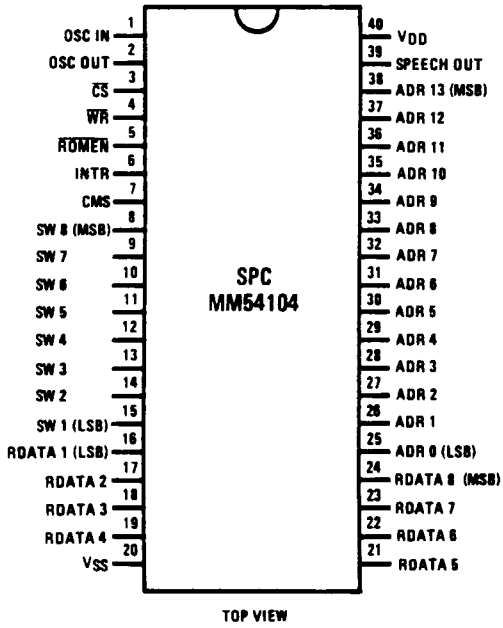


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

Block and Connection Diagrams



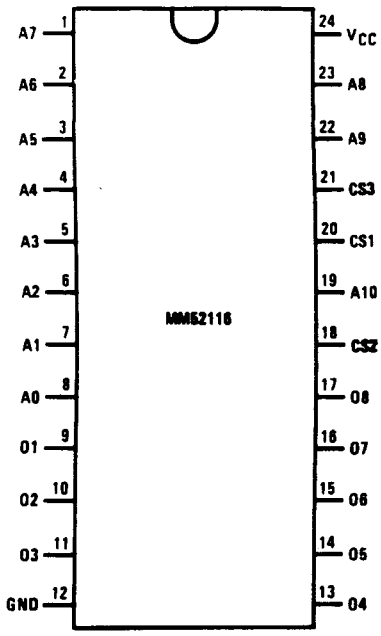
Dual-In-Line Package



TOP VIEW

Connection Diagrams (Continued) (V_{CC} = 4.75V–5.25V)

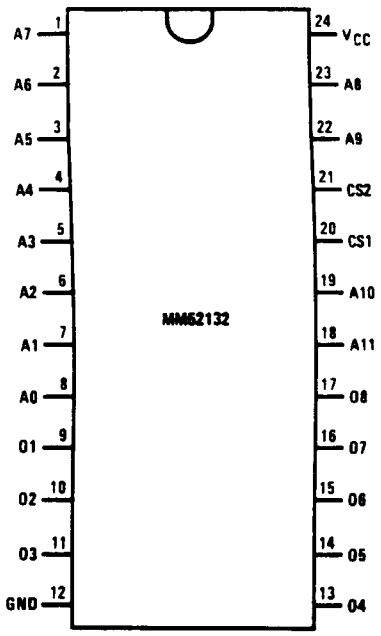
Dual-In-Line Package



TOP VIEW

16k

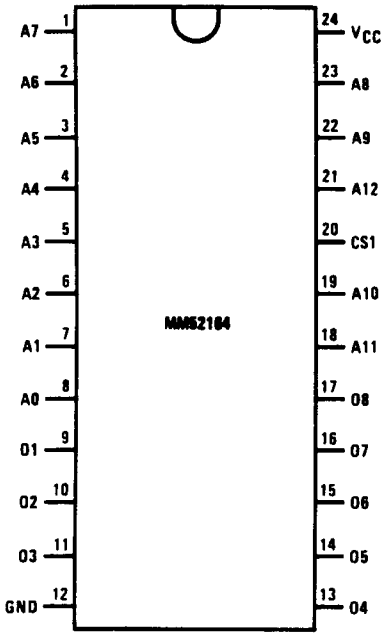
Dual-In-Line Package



TOP VIEW

32k

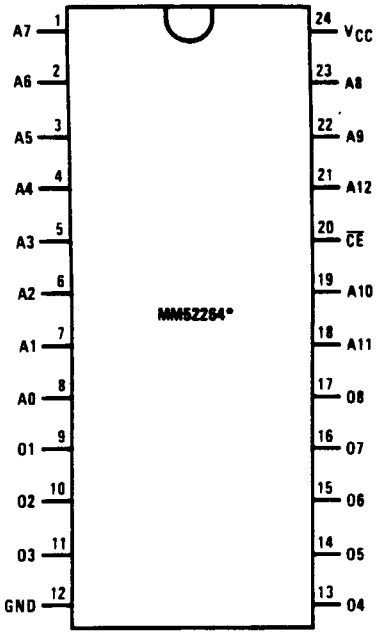
Dual-In-Line Package



TOP VIEW

64k

Dual-In-Line Package



TOP VIEW

*Future product

For specific ROM device information, see MM52116, MM52132, MM52164 or MM52264 data sheets.

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1-8): This is an 8-bit parallel data bus which contains the starting address of the speech data. Unused inputs must be tied to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW1-SW8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch is must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1-8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0-ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

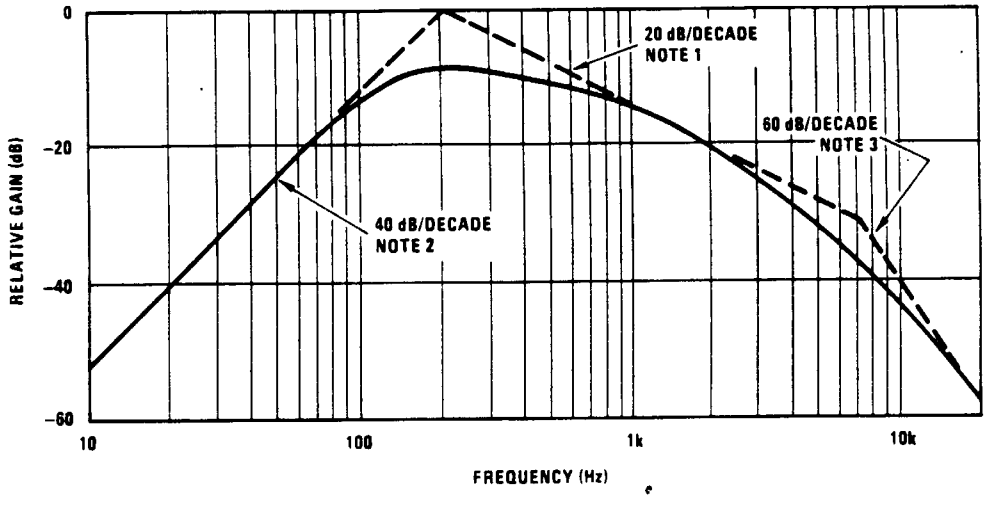
Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

Applications Information

Frequency Response of Combined Amplifier and Speaker



Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz-8000 Hz.